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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/640,961
Filing Date: August 16, 2000
Appellant(s): MA ET AL.

John N. Greaves

For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed January 7, 2011 appealing from the Office action mailed February 2, 2010.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:

Claims 1-4, 24-29, 31 and 33-40 are pending.

Claims 1-4, 24-29, 31 and 33-40 are rejected.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has a comment on the summary of claimed subject matter contained in the brief.

An inconsistency is created by appellant's referencing to Figures 2A-D for discussion of claim 26 subject matter. Nowhere in the cited drawings is the encapsulation material substantially coplanar with the dies' back surface. It is coplanar with the heat slug 152.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

3,407,479	Fordemwalt et al	10-1968
6,013, 953	Nishihara et al	1-2000
3,343,255	Donovan	09-1967
6,288,905	Chung	9-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung teaches in for example figures 6-8 a microelectronic package, comprising a microelectronic die 140 having an active surface and at least one side; encapsulation material 150 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and therefore obviously "planar to"); a first dielectric material layer 146 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 144 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 2, the microelectronic package of claim 1, further including at least one second dielectric material layer 120 disposed over said at least one first conductive trace and said first dielectric material layer.

With regard to claim 3, the microelectronic package of claim 2, wherein at least a portion of at least one second conductive trace 132b extends through and resides on said at least one second dielectric material layer.

With regard to claim 4, the microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 25, he microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die (see figure 7 where at least the left the bottom surface of encapsulant 150 is shown having a planar side surface running parallel to the planar back side surface of die 140 and therefore obviously" planar to").

Claims 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung shows a microelectronic package, comprising a microelectronic die having an active surface 140, a back surface, and at least one side; and encapsulation material 150 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface (see figure 7 where at least the bottom side surfaces

of encapsulant 150 are shown having a planar side surface running parallel to the back surface of die 140 and therefore obviously "planar to").

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace 140 (or 110 or 132a) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 28, the microelectronic package of claim 27, further including at least one second dielectric material layer (120) disposed over said at least one first conductive trace and said first dielectric material layer.

With regard to claim 29, the microelectronic package of claim 28, wherein at least a portion of at least one second conductive trace (132a) extends through and resides on said at least one second dielectric material layer.

Claims 31, 33, 34, 35 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung teaches in for example figures 6-8 and 14 microelectronic package, comprising: a plurality of microelectronic dice (see figure 14) each having an active surface and at least one side, encapsulation material 150 adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one surface substantially planar to said plurality of microelectronic dice active surfaces (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and therefore obviously "planar to") , and at least one first conductive trace disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace 144 extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 33, the microelectronic package of claim 31 further including at least one second dielectric material layer 120 disposed over said at least one first conductive trace and said first dielectric material layer.

With regard to claim 34, the microelectronic package of claim 33, wherein at least a portion of at least one second conductive trace 132a extends through and resides on said at least one second dielectric material layer.

With regard to claim 35, the microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device in thermal contact with said microelectronic die back surface.

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 37, the microelectronic package of claim 31, wherein the microelectronic die further includes a back surface, and wherein at least one surface of said encapsulation material is substantially planar to said microelectronic die active surface (see figure 7 where at least the top side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar active side surface of die 140 and therefore obviously" planar to").

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Fordemwalt et al.

Fordemwalt et al shows in for example figure 1 in microelectronic package, comprising: a microelectronic die 13 having an active surface and at least one side; encapsulation material 12 adjacent said at least one microelectronic die side, wherein

said encapsulation material includes at least one top surface shown substantially planar to said microelectronic die active surface; a first dielectric material layer 21 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace (25 or (22, 23, 24, 25) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface(see col. 4, lines 56-59), wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fordemwalt et al.

Fordemwalt et al shows in for example figure 1 a microelectronic package, comprising: a microelectronic die 13 having an active surface, a back surface, and at least one side; and encapsulation material 12 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface (see figure 1 where at least the bottom side surface of encapsulant 12 is shown having a planar side surface running parallel to the planar back side surface of die 13 and therefore obviously "planar to").

Though Fordemwalt et al fails to show a heat dissipation device in thermal contact with the back surface of the chip, thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art and a typical standard in this art. To therefore incorporate at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Fordemwalt et al

would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace (25 or (22, 23, 24, 25) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface (see col. 4, lines 56-59), wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claim 31 is rejected under 35 U.S.C. 102(b) as being anticipated by Fordemwalt et al.

Fordemwalt et al shows in for example figure 1 a microelectronic package, comprising: a plurality of microelectronic dice (13, 14, 15, 16) each having an active surface and at least one side, encapsulation material 12 adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one top surface substantially planar to said plurality of microelectronic dice active surfaces, and at least one first conductive trace (25 or (22, 23, 24, 25) disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface(see col. 4, lines 56-59) , wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

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Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Nishihara et al.

Nishihara shows in for example figure 3 (figure 7) a microelectronic package, comprising: a microelectronic die 1 having an active surface and at least one side; encapsulation material 8 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one bottom surface substantially planar to said microelectronic die active surface; a first dielectric material layer 3 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 2 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 26, 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishihara et al.

. Nishihara shows in for example figure 3 a microelectronic package, comprising: a microelectronic die 1 having an active surface, a back surface, and at least one side; and encapsulation material 8 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one bottom surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface.

Though Nishihara et al fails to show a heat dissipation device in thermal contact

with the back surface of the chip, thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art and a typical standard in this art to improve thermal dissipation. To therefore incorporate at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Nishihara et al would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace 4 disposed on said first dielectric material layer 3 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 1, 4, 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan.

Donovan shows a microelectronic package, comprising a microelectronic die 12b having an active surface and at least one side, encapsulation material 28 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface; 23 a first dielectric material layer disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 32 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first

conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claims 4, the microelectronic package of claim 1, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation device 40 thermal contact with said microelectronic device.

With regard to claim 24, the microelectronic package of claim 4, wherein said encapsulation material is shown adjacent at least a portion of said at least one heat dissipation device.

Claims 26, 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan.

Donovan shows a microelectronic package, comprising a microelectronic die 12b having an active surface, a back surface, and at least one side; and encapsulation material 28 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one top surface substantially planar to said microelectronic die active surface and at least one surface planar to said microelectronic die back surface and at least one heat dissipation device 40 is shown in thermal contact with said microelectronic die back surface.

With regard to claim 27, the microelectronic package of claim 26, further including at least one first conductive trace 32 disposed on said first dielectric material layer 23 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Claims 31, 35, 36 are rejected under 35 U.S.C. 102(b) as being anticipated by Donovan

Donovan shows a microelectronic package, comprising a plurality of microelectronic dice (12a, 12b, 12c) each having an active surface and at least one side, encapsulation material 28 adjacent said at least one microelectronic die side of said plurality of microelectronic dice, wherein said encapsulation material includes at least one top surface substantially planar to said plurality of microelectronic dice active surfaces, and at least one first conductive trace 32 disposed on said first dielectric material layer 23 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

With regard to claim 35, the microelectronic package of claim 31, wherein said microelectronic die further includes a back surface; and further including at least one heat dissipation 40 device in thermal contact with said microelectronic die back surface.

With regard to claim 36, the microelectronic package of claim 35, wherein said encapsulation material is shown adjacent at least a portion of said at least one heat dissipation device.

Claim 38 is rejected under 35 U.S.C. 102(b) as being anticipated by Donovan

Donovan shows a microelectronic package, comprising a microelectronic die 12b having an active surface, a back surface, and at least one side; encapsulation material 28 adjacent said at least one microelectronic die side, wherein said encapsulation

material includes at least one top surface substantially planar to said microelectronic die active surface; a first dielectric material layer 23 disposed on at least a portion of said microelectronic die active surface and said encapsulation, material surface; at least one first conductive trace 32 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface; and at least one heat dissipation device 40 in thermal contact with said microelectronic die back surface.

Claims 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung.

Chung teaches in for example figures 6-8 a microelectronic package, comprising: a microelectronic die 140 having an active surface and at least one side; encapsulation material 150 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface (see figure 7 where at least the left the side surface of encapsulant 150 is shown having a planar side surface running parallel to the planar side surface of die 140 and therefore obviously "planar to"); a first dielectric material layer 146 disposed on at least a portion of said microelectronic die active surface and said encapsulation material surface; and at least one first conductive trace 144 disposed on said first dielectric material layer and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace

extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface.

Thermal dissipation devices formed on the surfaces of chips and package structures are very well known in this art. To therefore incorporate at least one heat dissipation device in thermal contact with said microelectronic die back surface of the die of Chung would have been considered obvious to one having ordinary skill in this art for the purpose of improving thermal dissipation.

With regard to claim 39, the microelectronic package of claim 38, further including: at least one second dielectric material layer 120 disposed over said at least one first conductive trace and said first dielectric material layer, wherein at least a portion of at least one second conductive trace 132b extends through and resides on said at least one second dielectric material layer.

With regard to claim 40, the microelectronic package of claim 39, wherein said encapsulation material is adjacent at least a portion of said at least one heat dissipation device (see obvious above).

Claims 4, 24, 35, 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chung or Nishihara or Fordemwalt et al (as applied above) in view of Donovan et al.

The features of the claims from which claims 4, 24, 35, and 36 depend have been discussed in detail supra except for use of a heat dissipation device in thermal contact with the bottom surface of the microelectronic chip. Donovan teaches a similar device to those of Chung or Nishihara or Fordemwalt et al and teaches the use of heat dissipation device 40 formed in thermal contact with the back of microelectronic device 12c (12 a and 12b). Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to use a heat dissipation device on the bottom surface of the electronic device. The ordinary artisan would have been motivated to modify Chung or Nishihara or Fordemwalt for the purposes of improving or increasing heat dissipation. Further providing the bottom surfaces of electronic devices with heat dissipation structures to improve heat dissipation is well known and performed conventionally in this art.

Claims 1-4, 24-29, 31, 33-40 are rejected.

(10) Response to Argument

One of the primary issues argued by the applicant is that the prior art reference to Fordemwalt et al fails to teach "at least one conductive trace extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface" recited in for example claim one. Contrary to applicant's arguments, Fordemwalt et al clearly shows microelectronic die in the form of at least one transistor (see col. 4, lines 42,semiconductor devices (transistors) 13, 14, 15, 16 and figure one clearly shows each of said devices formed with a at least four sides including a top side where said trace is clearly shown. Trace is term known in this art as a conductive or metallization pattern formed on a substrate and may have various configurations. A trace may be an electrode or bond pad or other type of conductive interconnect pattern. Trace is defined for example in www.4pcb.com Advanced Circuits website **as** a segment of a conductor

route and in www.trianglecircuits.com Triangle Circuits website defines a trace as a layout or wiring of an electrical connection.

Applicant makes continuous references to a Harper packaging handbook but only provide references to areas where Harper seems label a component a trace but fails to provide a specific definition of the term trace rendered by Harper. Applicant's instant specification further fails to provide a specific definition of trace but shows various variations and configurations of trace 208, 234, 276 (shown in the prior art views) and 124, 132 each shown as a wiring segment or wiring pattern on a substrate.

Semiconductor device 13 (or device 16) of Fordemwalt taken as an example is shown to clearly have at least one trace 25, 26 (which is shown labeled in transistor 16) and col.4, lines 57-60 clearly teach the formation of traces where it states that "connectors (or traces) may be metalized over the surface of the oxide and through the openings of the… regions….to form the... circuit" and clearly rendering said traces adjacent said die active surface and adjacent the encapsulation material surface. Further the term "adjacent" fails to limit said trace to a specific area location but merely suggests "a vicinity" of the die surface and encapsulation material surface. Fordemwalt et al therefore clearly teaches the features of the invention as they are broadly recited, substantially item for item.

Another one of the primary issues argued by the applicant is relative to the prior art reference to Donavan whereby the alleged deficiencies of Donavan appear to be similar to the alleged deficiencies of Fordemwalt discussed above. Donovan teaches a similar device to that of Fordemwalt et al except that Donavan also teaches a heat dissipation device 40 in thermal contact with the back surface of the microelectronic device recited in claims 4, 26, 35, 36 and 38. Applicant argues that Donavan fails to teach a trace but only teaches an ohmic contact which the applicant argues is not a

trace. Col. 2, line 38 of Donovan teaches that ohmic contact and interconnects are formed on the surface of the die which are characteristics of traces whereby said contacts and interconnects are characteristic of segment of a conductor route or wiring of an electrical connection rendered in the definition above. The structural features shown by both Fordemwalt et al and Donovan are well known in semiconductor technology as surfaces of chip, dies, wafers, are typically formed with metalized surfaces which connect to active regions in the chip, die or wafers. Said metalized surfaces are commonly called terms such as interconnects or contacts whereby said terms may be also called traces.

Another one of the primary issues argued by the applicant is relative to the prior art reference to the Chung et al reference which the applicant alleges also fails to teach the features of the claimed invention and where Chung et al teaches the formation of a bump 144 and not a trace. Chung et al teaches that said bump 144 is formed integrated with an interconnect (trace) as shown by 26 in prior art figure 1 and figure 5 of Chung et al. In addition to what is taught in figures 6-8 of Chung et al, figure 14 of Chung et al shows die 140 having die sides adjacent to encapsulation 150, first dielectric material 120 disposed on the die, at least one trace 114a or 114b (having an integrated bump) disposed on the dielectric material and clearly shown in contact with the active surface of die 140 and adjacent to the die surface and the encapsulant material surface. Therefore figure 14 of Chung et al also teaches the features recited in the claims of the instant invention substantially item for item.

The final reference to Nishihara et al argued by the applicant also clearly teaches a trace 4 disposed on first dielectric 3 and in physical and electrical contact with the die active surface.

Applicant argues that Nishihara et al shows a bond pad which renders the trace of Nishihara not in physical contact with the die active surface. Said bond pad and trace of Nishihara are deemed to be integral structures necessary to provide contact to the active surface. Though the applicant takes issue with the structure of Nishihara said applicant shows a similar bond pad structure in the figures of the instant invention in for example figures 1f, 1g, 1j, 2d all show bond pad 108 connected to the at least one trace 124. So the trace of the applicant's instant invention is also utilized in conjunction with a bond pad 108. NIshihara et al also clearly deemed to teach the features of the invention of which the rejection of directed.

Other aspects recited in the claims such as the use of heat dissipation or heat sinks attached to the back surfaces of chips to provide for heat dissipation are commonly performed in this art and the reference of Donavan has been used to show the well known use of heat dissipation devices attached to semiconductor devices (i.e. microelectronic dies). It is further well known to form a plurality of dielectric layers on the surfaces of chips having metalization or traces formed thereon. Die surface are typically formed with alternating metal and dielectric multilayered structures.

Lastly the applicant has failed to recite structure that is inventive relative what is currently expressed in the claims of the instant invention whereby the features recited in the instant claims are not only taught by the prior art references relied upon in the rejections but these features are clearly admitted by the applicant as being well known in this technology where he teaches in prior art figure 10 of the instant disclosure, a microelectronic die 256 having an active surface and at least one side; encapsulation material 264 adjacent said at least one microelectronic die side, wherein said encapsulation material includes at least one surface substantially planar to said microelectronic die active surface; a first dielectric material layer 252 disposed on at least a portion of said microelectronic die active surface and said encapsulation material

surface; and at least one first conductive trace 272 disposed on said first dielectric material layer 252 and in physical and electrical contact with said microelectronic die active surface, wherein said at least one first conductive trace 272 (connected to contact 266) extends adjacent said microelectronic die active surface and adjacent said encapsulation material surface. Even applicant's prior art figure teaches the features recited in the instant claims to be well known prior art.

It is deemed that the references relied upon in the rejection are proper to teach the features as they are broadly recited in the claims of the instant invention substantially item for item relative to many of the claims recited. Applicant by his own admission as also taught these features to be conventional as is known in his prior art figure 10. Other features recited in the instant claims such as the use of heat sinks and multilayer structure that have been discussed in the rejections and arguments above are deemed to also be conventional structure typically provided with microelectronic device structure and very well known to one having ordinary skill in this technology.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/S. V. Clark/

Primary Examiner, Art Unit 2823

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